Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of the claims in the application:

1-12. (Cancelled).

13. (Currently Amended) A computer-implemented method of scheduling processing in a hardware threaded circuit, comprising:

in a processor, receiving inputs corresponding to unthreaded processing of an application;

receiving and storing in a memory information including processing element resources, a number of processing elements, and a window size corresponding to a number of downstream processing states to be examined; [[and]]

generating a hardware threaded schedule for processing the application with at least first and second one of the processing elements being interconnected to enable dynamic resource sharing;

synthesizing the hardware threaded schedule to an Application Specific Circuit (ASC); and

synthesizing the hardware schedule to maximize throughput.

14. (Canceled)

15. (Canceled)

16. (Currently Amended) The method according to claim [[14]] 13, further including synthesizing the hardware threaded schedule to reduce power consumption.

17. (Original) The method according to claim 13, further including receiving resource constraint information for the processing elements.

18. (Currently Amended) A hardware threaded circuit system, comprising:

an input to receive inputs corresponding to unthreaded processing of an application;

a memory to store information including processing element resources, a number of processing elements, and a window size corresponding to a number of downstream processing states to be examined;

a task manager coupled to the memory for synthesizing a hardware threaded schedule to an Application Specific Circuit (ASC) and maximizing throughput; and

a plurality of the processing elements coupled to the task manager, wherein first and second ones of the plurality of processing elements are interconnected for hardware threaded processing to enable dynamic borrowing of processing resources associated with the second one of the plurality of processing elements by the first one of the plurality of processing elements.

19. (Canceled)

20. (Original) The system according to claim 18, wherein the circuit reduces power consumption compared to a non-threaded processing for substantially similar system wait times.

21. (Original) The system according to claim 18, wherein the first and second processing elements each include a first type of resource and a second type of resource and a multiplexer such that the interconnection includes at least one input signal being provided to the first type of resource in the first and second processing elements.

22. (Original) The system according to claim 21, wherein the interconnection includes a connection from an output of the second processing element first type of resource to the first processing element.

23. (Previously Presented) The method of claim 13, wherein the at least first and second one of the processing elements are multiplexed.